CLAIMS

What is claimed is:

1. An apparatus for communicating global link control words (LCW) between chips, said apparatus comprising:

a queue for storing an LCW, said queue having in input for receiving an LCW from a previous chip, and an output for outputting a stored LCW to a subsequent chip;

a management circuit for comparing an incoming LCW with a previously stored LCW; and

a combiner circuit for combining the incoming LCW with a previously stored LCW and storing the combined LCW in said queue when said management circuit determines that the incoming LCW can be combined with the previously stored LCW.

2. The apparatus according to claim 1 wherein said queue has multiple elements, and said combiner circuit stores said incoming LCW in a separate queue element when said management circuit determines the incoming LCW cannot be combined with the previously stored LCW.

3. The apparatus according to claim 1 wherein each LCW comprises bits and said combiner circuit comprises an OR circuit for combining the bits of said incoming LCW with the bits of said previously stored LCW.

4. The apparatus according to claim 3 wherein a selected bit of each LCW, when in a certain state, indicates that the LCW cannot be combined with another LCW, and said management circuit interrogates the state of said selected bit of said incoming LCW.

5. The apparatus according to claim 3 wherein at least two selected bits of said LCWs have an Exclusive OR relationship wherein either of the bits may be on, but not both, and said management circuit controls the combiner circuit such that two LCWs will not be combined if the Exclusive OR relationship is violated.

6. A method for communicating global link control words (LCW) between chips, said method comprising:

storing an LCW in a queue, said queue having in input for receiving an LCW from a previous chip, and an output for outputting a stored LCW to a subsequent chip;

comparing an incoming LCW with a previously stored LCW; and

combining the incoming LCW with a previously stored LCW and storing the combined LCW in said queue when said management circuit determines that the incoming LCW can be combined with the previously stored LCW.

7. The method according to claim 6 further comprising storing in a separate element of said queue, said incoming LCW when it is determined in said determining step that the incoming LCW cannot be combined with the previously stored LCW.

8. The method according to claim 6 wherein each LCW comprises bits and said combining step comprises combining the bits of said incoming LCW with the bits of said previously stored LCW with an OR circuit.

9. The method according to claim 8 wherein a selected bit of each LCW, when in a certain state, indicates that the LCW cannot be combined with another LCW, and said comparing step comprises interrogating the state of said selected bit of said incoming LCW.

10. The method according to claim 8 wherein at least two selected bits of said LCWs have an Exclusive OR relationship wherein either of the bits may be on, but not both, and said combining step comprises preventing the combining of two LCWs if the Exclusive OR relationship is violated.

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